What is claimed is:

1. A bipolar transistor comprising:

a collector selected from one or more of the group SiC, (4H, 6H, 15R, 3C....);

a base selected from one or more of the group Si, Ge and SiGe; and

an emitter selected from one or more of the group Si, SiGe, SiC, amorphous-Si, amorphous-SiC and diamond-like carbon.

2. The bipolar transistor of claim 1 wherein at least one of a first interface between said collector and said base and a second interface between said base and said emitter is a direct-wafer-bonded interface.

3. The bipolar transistor of claim 1 including:

a sub-collector selected from one or more of the group SiC, (4H, 6H, 15R, 3C....).

4. The bipolar transistor of claim 3 wherein at least one of a first interface between said collector and said base, a second interface between said base and said emitter, and a third interface between said collector and said sub-collector is a direct-wafer-bonded interface.

5. The bipolar transistor of claim 1 wherein said emitter is Si, said base is Si, and said collector is SiC.

6. The bipolar transistor of claim 5 wherein at least one of a first interface between said SiC collector and said Si base and a second interface between said Si base and said Si emitter is a direct-wafer-bonded interface.

7. The bipolar transistor of claim 5 including:

a SiC sub-collector.

8. The bipolar transistor of claim 7 wherein at least one of a first interface between said SiC sub-collector and said SiC collector, a second interface between said SiC collector and said Si base, and a third interface between said Si base and said Si emitter is a direct-wafer-bonded interface.

9. The bipolar transistor of claim 1 wherein said emitter is Si, said base is Ge, and said collector is SiC.

10. The bipolar transistor of claim 9 wherein at least one of a first interface between said SiC collector and said Ge base and a second interface between said Ge base and said Si emitter is a direct-wafer-bonded interface.

11. The bipolar transistor of claim 10 including:

a SiC sub-collector.

12. The bipolar transistor of claim 11 wherein at least one of a first interface between said SiC sub-collector and said SiC collector, a second interface between said SiC collector and said Ge base, and a third interface between said Ge base and said Si emitter is a direct-wafer-bonded interface.

13. The bipolar transistor of claim 1 wherein a bandgap of said collector and a bandgap of said emitter are larger than a bandgap of said base.

14. The bipolar transistor of claim 13 wherein at least one of a first interface between said collector and said base and a second interface between said base and said emitter is a direct-wafer-bonded interface.

15. The bipolar transistor of claim 14 including:

a sub-collector selected from one or more of the group SiC and SiC polytypes (4H, 6H, 3C, 15R...).

16. The bipolar transistor of claim 15 wherein at least one of a first interface between said collector and said base, a second interface between said base and said emitter, and a third interface between said collector and said sub-collector are a direct-wafer-bonded interface.

17. A method of making a heterojunction bipolar transistor, comprising the steps of:

providing an emitter/base layer having a generally flat base-surface;

providing that said emitter/base layer includes an emitter portion selected from one or more of the group Si, SiGe, SiC, amorphous-Si, amorphous-SiC and diamond-like carbon, and a base-portion selected from one or more of the group Si, Ge and SiGe;

providing that said base portion includes a generally flat base surface;

processing said base-surface to produce a base-surface that is compatible with direct-wafer-bonding;

providing a collector layer;

providing that said collector layer is selected from one or more of the group SiC, (4H, 6H, 15R, 3C.....);

providing that said collector layer includes a generally-flat collector-surface;

processing said collector-surface to produce a collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said base-surface to said collector-surface.

18. The method of claim 17 including the steps of:

providing that said collector layer includes a second-surface that extends generally parallel to said collector-surface;

processing said second-surface to produce a second-surface that is compatible with direct-wafer-bonding;

providing a sub-collector layer having a generally flat sub-collector-surface;

processing said sub-collector-surface to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said second-surface to said sub-collector-surface.

19. The method of claim 17 including the steps of:

providing that said emitter/base layer includes the number of emitter-portions, each having an emitter-surface that is compatible with direct-wafer-bonding;

providing a number of physically spaced base-portions, each having a base-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding each individual one of said emitter surfaces to an individual one of said base-surfaces.

20. The method of claim 19 including the steps of:

providing that said collector layer includes a second-surface that extends generally parallel to said collector-surface;

processing said second-surface to produce a second-surface that is compatible with direct-wafer-bonding;

providing a sub-collector layer having a generally flat sub-collector-surface;

processing said sub-collector-surface to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said second-surface to said sub-collector-surface.

21. The method of claim 14 including the steps of:

providing that said emitter/base layer includes an emitter-portion and a base-portion; and

providing that a bandgap of said emitter-portion and a bandgap of said collector layer are larger than a bandgap of said base-portion.

22. The method of claim 21 including the steps of:

providing that said collector layer includes a second-surface that extends generally parallel to said collector-surface;

processing said second-surface to produce a second-surface that is compatible with direct-wafer-bonding;

providing a sub-collector layer having a generally flat sub-collector-surface;

processing said sub-collector-surface to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said second-surface to said sub-collector-surface.

23. A bipolar transistor comprising:

a collector selected from the group SiC and SiC polytypes (4H, 6H, 15R, 3C...), said collector having a collector-surface;

a base selected from the group Si, Ge and SiGe, said base having a first base-surface engaging said collector-surface, and said base having a second base-surface;

at least a first emitter selected from the group Si, SiGe, SiC, amorphous-Si, amorphous-SiC and diamond-like carbon engaging said second base-surface: and

at least a second emitter selected from the group Si, SiGe, SiC, amorphous-Si, amorphous-SiC and diamond-like carbon, said second emitter being spaced from said at least a first emitter, and said at least a second emitter engaging said second base-surface.

24. The bipolar transistor of claim 23 wherein at least one of a first interface between said collector-surface and said first base-surface, a second interface between said second base-surface and said at least a first emitter, and a third interface between said second base-surface and said at least a second emitter is a direct-wafer-bonded interface.

25. The bipolar transistor of claim 23 wherein a bandgap of said collector, a bandgap of said at least a first emitter and a bandgap of said at least a second emitter are larger than a bandgap of said base.

26. The bipolar transistor of claim 25 wherein at least one of a first interface between said collector-surface and said first base-surface, a second interface between said second base-surface and said at least a first emitter, and a third interface between said second base-surface and said at least a second emitter is a direct-wafer-bonded interface.

27. A heterojunction comprising:

a first semiconductor layer selected from the group Si and Si_1Ge_{1-x};

said first semiconductor layer having a top surface and a bottom surface;

a first SiC layer;

said first SiC layer having a top surface and a bottom surface; and

a direct-wafer-bonded interface between said bottom surface of said first semiconductor layer and said top surface of said SiC layer.

28. In combination with the heterojunction of claim 27:

a Si layer;

said Si layer having a top surface and a bottom surface; and

a direct-wafer-bonded interface between said top surface of said first semiconductor layer and said bottom surface of said Si layer.

29. In the combination of claim 28:

a second SiC layer;

said second SiC layer having a top surface and a bottom surface; and

a direct-wafer-bonded interface between said bottom surface of said first SiC layer and said top surface of said second SiC layer.